L8: Entry 2 of 3 File: USPT Feb 1, 2000

DOCUMENT-IDENTIFIER: US 6021513 A
TITLE: Testable programmable gate array and associated LSSD/deterministic test methodology

Detailed Description Text (21):
The interconnect associated with the receiver inhibit signal RI provides a direct control input for inhibiting certain receivers of the FPGA. DI1 and DI2 provide direct control of certain drivers associated with the FPGA. The interconnect associated with the MUX test control signal C.sub.-- TEST provides a direct input for enabling testing of certain passgate multiplexers of the FPGA. Similarly, direct inputs CONFG and REPT enable operation of configuration scan chain 24 and repeater latch scan chains 30 respectively. The remaining test ports of the expanded interface are associated with-scanning data into, or out of, the various repeater scan chains and configuration scan chains, and providing additional LSSD clocks for clocking the configuration scan chain.

Detailed Description Text (37):
FIG. 7a provides a timing diagram associated with operating the I/O boundary scan chain, wherein the portion thereof associated with the control register 28 is in series with I/O ring portion 58. During this operating sequence, it is assumed that the expanded test interface control signal TESTMORE, the bypass control signal BP, and the boundary scan steering control signal CNTL are all inactive. Accordingly, multiplexer 56 (FIG. 6) selects the serial output of I/O ring portion 58 as the serial input to the last register 48, and multiplexer 54 selects data from the serial output of the last register 48 of the I/O boundary scan chain as the serial output SO of the FPGA. The timing diagram consists of three intervals 200, 202 and 204. During interval 200, data is serially loaded into the I/O boundary scan chain by a sequence of LSSDA and LSSDB clock pairs. After serially loading the I/O boundary scan chain, a subsequent pulse "N" of MTEST updates control register 28 in accordance with the data of the associated cells of the I/O boundary scan chain 26.

Detailed Description Text (79):
Next, the I/O ports of the FPGA are tested per their default configurations. The I/O ports are programmable in accordance with configuration data as stored in associated locations of SRAM 14. At power on, SRAM 14 is initiated to a known reset condition. Accordingly, the I/O ports of the FPGA are in their default configurations. As described hereinbefore, the multiplexers associated with the cells of the I/O boundary scan chain 26 are controlled by the transmit and receiver control signals, PT0 and PR0 respectively, as provided by control register 28. At power on, each of these control signals are set to a known default condition. Likewise, the receiver and driver inhibit control signals (RI, DI1, and DI2) also provided by control register 26, provide default power-on values as necessary for testing the default configurations of the I/O ports. The multiple-use I/O ports "m" are kept in their functional settings by holding the expanded test interface control signal TESTMORE high. Accordingly, the I/O boundary scan chain is employed for testing the functionality of the functional I/O ports, including the boundary scan "bs" and multiple-use ports "m" as listed in Table 1, per their default configurations.

L8: Entry 3 of 3 File: USPT Feb 2, 1999

DOCUMENT-IDENTIFIER: US 5867507 A
** See image for Certificate of Correction **
TITLE: Testable programmable gate array and associated LSSD/deterministic test methodology

Detailed Description Text (20):
The interconnect associated with the receiver inhibit signal RI provides a direct control input for inhibiting certain receivers of the FPGA. DI1 and DI2 provide direct control of certain drivers associated with the FPGA. The interconnect associated with the MUX test control signal C.sub.-- TEST provides a direct input for enabling testing of certain passgate multiplexers of the FPGA. Similarly, direct inputs CONFG and REPT enable operation of configuration scan chain 24 and repeater latch scan chains 30 respectively. The remaining test ports of the expanded interface are associated with scanning data into, or out of, the various repeater scan chains and configuration scan chains, and providing additional LSSD clocks for clocking the configuration scan chain.

Detailed Description Text (36):
FIG. 7a provides a timing diagram associated with operating the I/O boundary scan chain, wherein the portion thereof associated with the control register 28 is in series with I/O ring portion 58. During this operating sequence, it is assumed that the expanded test interface control signal TESTMORE, the bypass control signal BP, and the boundary scan steering control signal CNTL are all inactive. Accordingly, multiplexer 56 (FIG. 6) selects the serial output of I/O ring portion 58 as the serial input to the last register 48, and multiplexer 54 selects data from the serial output of the last register 48 of the I/O boundary scan chain as the serial output SO of the FPGA. The timing diagram consists of three intervals 200, 202 and 204. During interval 200, data is serially loaded into the I/O boundary scan chain by a sequence of LSSDA and LSSDB clock pairs. After serially loading the I/O boundary scan chain, a subsequent pulse "N" of MTEST updates control register 28 in accordance with the data of the associated cells of the I/O boundary scan chain 26.

Detailed Description Text (77):
Next, the I/O ports of the FPGA are tested per their default configurations. The I/O ports are programmable in accordance with configuration data as stored in associated locations of SRAM 14. At power on, SRAM 14 is initiated to a known reset condition. Accordingly, the I/O ports of the FPGA are in their default configurations. As described hereinbefore, the multiplexers associated with the cells of the I/O boundary scan chain 26 are controlled by the transmit and receiver control signals, PT0 and PR0 respectively, as provided by control register 28. At power on, each of these control signals are set to a known default condition. Likewise, the receiver and driver inhibit control signals (RI, DI1, and DI2) also provided by control register 26, provide default power-on values as necessary for testing the default configurations of the I/O ports. The multiple-use I/O ports "m" are kept in their functional settings by holding the expanded test interface control signal TESTMORE high. Accordingly, the I/O boundary scan chain is employed for testing the functionality of the functional I/O ports, including the boundary

scan "bs" and multiple-use ports "m" as listed in Table 1, per their default configurations.

Previous Doc Next Doc Go to Doc#

L8: Entry 1 of 3 File: USPT Apr 22, 2003

DOCUMENT-IDENTIFIER: US 6552410 B1
TITLE: Programmable antifuse interfacing a programmable logic and a dedicated device

Detailed Description Text (28):
Test circuitry similar to that shown in FIG. 7 can also be used to test buffers conveying signals from the dedicated logic to the programmable logic. Further, the two kinds of buffers could be connected in the same scan chain or separate scan chains for testing. FIG. 8 is a simplified diagram showing an interface buffer circuit 100 that receives a signal FPGA in from programmable logic 12 and generates a signal PCIout to dedicated logic 14 and an interface buffer 110 that receives a signal PCIin from dedicated logic 14 and generates a signal FPGAout to programmable logic 12. Interface buffer circuit 100 includes an input multiplexer 103, a NAND gate 102, an inverter 104, and transistors 106 and 108 that operate in the manner described above for similarly-numbered elements. Signals con0b and Datain of FIG. 8 correspond to signals EN[i] and T[i] in FIG. 7.